1. A method of decoding errors occurring in data stored in memory, comprising:

applying data to be stored in a buffer memory to a generator matrix to generate parity check bits;

storing the parity check bits in the buffer memory following the data;

reading the stored data and parity check bits;

regenerating the parity check bits; and

producing from the stored and regenerated parity check bits a result that is usable to directly identify a location of an erroneous bit of the data in the buffer memory.

2. The method of claim 1 wherein the result is in the form of a syndrome.

3. The method of claim 1 wherein the data are stored in buffer locations in the buffer memory, and the location comprises an address of one of the buffer locations.

4. The method of claim 3 wherein the location further comprises a bit position within the buffer location.

5. The method of claim 1 wherein the generator matrix comprises a data portion and a parity check generation portion, and the parity check generation portion comprises rows of bits corresponding to binary representations of the buffer locations used to store the data.

6. The method of claim 5 wherein the parity check generation portion of the generator matrix comprises columns of bit sequences usable to select combinations of data bits for parity check bit generation, each column corresponding to a different parity check bit.

7. The method of claim 6 wherein the generator matrix has a minimum distance of three and describes an error correction code with single-bit error correction capability.

8. The method of claim 7 wherein one of the columns is usable to generate a parity-on-parity check bit.

9. The method of claim 7 wherein one of the columns is usable to select data parity in producing a parity check bit.

10. The method of claim 6 wherein the generator matrix has a minimum distance of four and describes an error correction code with single-bit error correction capability.

11. The method of claim 10 wherein the columns comprise a column to select data parity in producing a parity check bit and a column to generate a parity-on-parity check bit.

12. The method of claim 6 wherein the generator matrix has a minimum distance of five and describes an error correction code with a double-bit error correction capability, and wherein producing comprises:

producing from the stored and regenerated parity check bits a result that is usable to directly identify locations of two erroneous bits of the data in the buffer memory.

13. The method of claim 12 wherein the rows of the parity check generation portion comprise bits corresponding to a first field element and a second field element, and wherein the second field element has the same properties as the first field element.

14. The method of claim 13 wherein the second field element is generated from the first field element.

15. The method of claim 13 wherein the second field element is generated from the first field element by a cyclic rotation of bits in the first field element.

16. The method of claim 13 wherein the first and second field elements are field elements of a Galois field of $GF(2^p)$, where p is an integer.

17. The method of claim 16 wherein the first element comprises a binary

representation β^k and the second element comprises a binary representation β^{sk} where k is an integer in a range of 1 to 2^p-1 and s does not divide 2^p-1.

18. The method of claim 17 wherein the integer p is equal to 14.

19. The method of claim 18 wherein s is equal to 5.

20. The method of claim 17 wherein the two erroneous bits are associated with ones of the first and second elements, and the first and second elements provide the locations of the two erroneous bits.

21. The method of claim wherein the first element comprises a binary representation β^k and the second element comprises a binary representation β^{-k} where k is an integer in a range of 1 to 2^p-1.

22. The method of claim 14 wherein the first element comprises a normal basis representation of a binary number.

23. An encoding method comprising:

applying data to be stored in a buffer memory to a generator matrix to generate parity check bits, the generator matrix comprising a data portion and a parity check generation portion, and the parity check generation portion comprises rows of bits corresponding to binary representations of the buffer locations to be used to store the

data;

storing the data in the buffer memory at the buffer locations; and

storing the parity check bits in the buffer memory following the data.

24. A data storage system comprising:

a storage medium;

a controller coupled to the storage medium; and

a buffer memory coupled to the storage medium and the controller for storing data to be written to the storage medium and data read from the storage medium;

wherein the controller is operable to perform the following steps:

applying data to be stored in a buffer memory to a generator matrix to generate parity check bits;

storing the parity check bits in the buffer memory following the data;

reading the stored data and parity check bits;

regenerating the parity check bits; and

producing from the stored and regenerated parity check bits a result that is usable to directly identify a location of an erroneous bit of the data in the buffer memory.

25. A data storage system comprising:

a storage medium;

a controller coupled to the storage medium; and

a buffer memory coupled to the storage medium and the controller for storing data to be written to the storage medium and data read from the storage medium;

wherein the controller is operable to perform the following steps:

applying data to be stored in the buffer memory to a generator matrix to generate parity check bits, the generator matrix comprising a data portion and a parity check generation portion, and the parity check generation portion comprises rows of bits corresponding to binary representations of the buffer locations to be used to store the data;

storing the data in the buffer memory at the buffer locations; and

storing the parity check bits in the buffer memory following the data.

26. An apparatus comprising:

a controller coupled to a storage medium; and

a buffer memory coupled to the controller for storing data to be written to the storage medium and data read from the storage medium;

wherein the controller is operable to perform the following steps:

applying data to be stored in a buffer memory to a generator matrix to generate parity check bits;

storing the parity check bits in the buffer memory following the data;

reading the stored data and parity check bits;

regenerating the parity check bits; and

producing from the stored and regenerated parity check bits a result that is usable to directly identify a location of an erroneous bit of the data in the buffer memory.

27. An apparatus comprising:

a controller coupled to a storage medium; and

a buffer memory coupled to the controller for storing data to be written to the storage medium and data read from the storage medium;

wherein the controller is operable to perform the following steps:

applying data to be stored in the buffer memory to a generator matrix to generate parity check bits, the generator matrix comprising a data portion and a parity check generation portion, and the parity check generation portion comprises rows of bits corresponding to binary representations of the buffer locations to be used to store the data;

storing the data in the buffer memory at the buffer locations; and

storing the parity check bits in the buffer memory following the data.